

**I/O CIRCUIT USING LOW VOLTAGE TRANSISTORS WHICH CAN  
TOLERATE HIGH VOLTAGES EVEN WHEN POWER SUPPLIES ARE  
POWERED OFF**

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**CROSS-REFERENCE TO RELATED APPLICATIONS**

**[0001]** This application is a continuation-in-part of Application No. 10/043,788, filed January 9, 2002, which claims the benefit of U.S. Provisional Application No. 60/260,580, filed January 9, 2001, and U.S. Provisional Application No. 60/260,582, filed January 9, 2001, all three of which are hereby incorporated by reference in their entirety; and this application also claims the benefit of U.S. Provisional Application No. 60/427,954, filed November 21, 2002, which is hereby incorporated by reference in its entirety.

**BACKGROUND OF THE INVENTION**

**Field of the Invention**

**[0002]** The present invention relates to integrated circuits (ICs), such as interface circuits, that are designed having reduced feature sizes, for example, 0.13  $\mu\text{m}$ . More particularly, the invention relates to ICs that include interfaces (such as input/output (I/O) circuits) that are capable of interfacing with comparatively high-voltage signals from other sources, for example a 3.3 volt IC interfacing with signals from a 5 volt IC, or any other disparate ranges. Moreover, the invention relates to integrated circuits in which the semiconductor devices are biased such that the stress across the gate-oxides and junctions, as well as the leakage currents, are maintained at tolerable levels.

## Related Art

[0003] The trend in CMOS-based processing technology is to produce integrated circuit (IC) cores having a higher density of semiconductor devices, such as transistors, and faster clock rates than their predecessors. I/O circuits, which electrically couple an IC core to external components, are accessed through I/O circuit pads that surround the IC core. The IC core and the I/O circuit pads are generally fabricated from the same processing technology. There is however no requirement that they comprise the same technology and hybrid circuits are known in the art. The inventive concepts herein are applicable to a variety of fabrication technologies.

[0004] The performance of the IC cores may generally be improved by shrinking the feature sizes of the semiconductor devices, for example field-effect transistors (FETs). Unfortunately, reducing the IC feature sizes may proportionally decrease the maximum operating voltage that the semiconductor devices within the IC can withstand. For example, an I/O circuit pad, fabricated from a CMOS process having 0.30 micron features, typically withstands a maximum operating voltage of about 3.6 volts. In such a case the maximum operating voltage of the I/O circuit pad is insufficient to drive the external components which have a higher voltage requirement, such as 5 volts. Furthermore, if the IC is interfaced with a greater than the maximum operating voltage, the IC may fail.

[0005] One way to attempt to resolve such requirements of circuits with mismatched voltage requirements is to increase the robustness of the fabrication process, for example by increasing the thickness of the gate-oxide layer of the semiconductor devices which comprise the IC circuitry. A thick gate-oxide layer may provide semiconductor devices, such as FETs, with the ability to support a higher voltage requirement. However, this voltage robustness is commonly accompanied by a decrease in the performance of the IC, because the thick gate-oxide layer reduces the overall gain of the devices

which comprise the IC. Reducing the gain minimizes the benefit which occurs by reducing the feature size.

[0006] Other attempts have included increasing the complexity of the CMOS fabrication process so there are multiple sets of devices where each set meets different voltage requirements. Each set of devices requires a different gate-oxide. Each additional gate-oxide requires a separate mask. The resulting hybrid process may significantly increase the manufacturing costs of the IC.

[0007] One way to avoid the drawbacks of the aforementioned processing-based solutions is to use a "level-shift" chip as an external component. The IC core and the I/O circuits are fabricated from the same process. The "level-shift chip" may be fabricated from a process that supports the discrete voltage requirement by stepping up the core output signals to support the discrete voltage range and stepping down the external drive signals to support the IC core voltage range. Such a level-shift chip can be a waste of much needed space on a crowded printed circuit board and may degrade performance.

[0008] An I/O circuit that transforms voltages between different voltage levels without degrading the overall performance of the integrated circuit and maximizing use of space on the printed circuit board or multi-chip substrate may be beneficial. It would be a further benefit if such an I/O circuit could use voltages presented at the I/O circuit in order to provide such protective biasing.

[0009] Commonly an I/O power supply may vary +/- 10% and may vary significantly more during transient conditions. When the I/O power supply varies, circuits may have higher stress on the gate-oxides of the devices in the I/O circuit, such stresses may not be desirable in many process technologies. It would be desirable to provide bias voltages to various devices in the I/O circuit such that the device gate-oxide is protected from high-voltages under various conditions of operation even when the power-supply voltage varies by a large amount, or when the power-supplies are powered off.

[0010] Embodiments of the present invention may be optimized, for example where 5 volt input tolerance is required, even when the power supplies are varying in steady state by +/- 10%, or are powered off.

[0011] Embodiments of the present invention are illustrated in an optimized form for I/O circuits where a 5 volt +/- 10% input tolerance is required for normal operating range. Additionally the inventive concepts herein are described in terms of CMOS (Complimentary Metal Oxide Semiconductor) integrated circuits. Those skilled in the art will readily appreciate the fact that techniques described with respect to CMOS ICs are readily applicable to any circuits having disparate power supply and/or drive signal requirements for different portions of the circuitry. The CMOS example chosen is one likely to be familiar to those skilled in the art. There is, however, no intent to limit the inventive concepts to CMOS ICs as the techniques are equally applicable to a wide variety of integrated circuit fabrication techniques.

#### SUMMARY OF THE INVENTION

[0012] An exemplary embodiment of the invention includes an integrated circuit having a four device input output circuit in a push pull configuration. Two of the devices, termed upper devices, comprise PMOS (P-Channel Metal Oxide Semiconductor) devices and two of the devices, termed lower devices, comprise NMOS (N-channel Metal Oxide Semiconductor) devices. The devices are biased to eliminate hazardous voltages across device junctions and to reduce the magnitude of the voltage being passed on to the core circuitry. The biases are derived from the input output state of the circuit, a plurality of power supply voltages, and the voltage presented to the I/O circuit connection ( $V_{PAD}$ ). Additionally PMOS device well bias voltage may be developed based on  $V_{PAD}$ . In a particular embodiment, the bias will be maintained even when the plurality of reference voltages are powered off, as is the case in power management mode.

[0013] An apparatus for providing bias voltages for input/output (I/O) connections on low voltage integrated circuits is disclosed. In one embodiment, the invention comprises an I/O pad, a pull-down transistor device that has a protective transistor coupled to said I/O pad, and a pull-up transistor device that has a second protective transistor, coupled to said I/O pad. A first switch coupled to the first protective transistor is responsive to a first supply voltage, a second supply voltage, and a reference voltage. Likewise, a second switch coupled to the second protective transistor is responsive to the first supply voltage and the reference voltage. A first self-bias circuit is also coupled to the first switch, wherein said the self-bias circuit uses a voltage at said I/O pad to bias the first protective transistor when both of the first and second supply voltages are powered off. Likewise, a second self-bias circuit coupled to the second switch, wherein the second self-bias circuit also uses the voltage at the I/O pad and an output of the first self bias circuit, to bias the second protective transistor when the first supply voltage is powered off.

#### BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

- [0014] Other features and advantages of the invention will become apparent from a description of the following figures, in which like numbers refer to similar items throughout.
- [0015] Figure 1 is a graphic illustration of an exemplary environment in which embodiments of the invention may be utilized.
- [0016] Figure 2 is a graphical illustration of a prior art input output circuit and connection.
- [0017] Figure 3 is a schematic of a portion of a CMOS (Complimentary Metal Oxide Semiconductor) input output circuit in which single push pull output devices, as illustrated in figure 2, have been replaced by two devices each.
- [0018] Figure 4 is an input output circuit, including a well biasing circuit, according to an embodiment of the invention.

- [0019] Figure 5 is a graph illustrating the relationship between well voltage and I/O pad voltage for the input (or a tristate) mode, according to an embodiment of the invention.
- [0020] Figure 6 is a block diagram of I/O circuitry biasing according to an embodiment of the invention.
- [0021] Figure 7 is a graphical representation of a bias voltage ( $V_{GP1}$ ) as a function of I/O pad voltage ( $V_{PAD}$ ), according to an embodiment of the invention.
- [0022] Figure 8 is a graphical illustration of a portion of a circuit configuration used to provide the I/O pad voltage to the core circuitry, according to an embodiment of the invention.
- [0023] Figure 9A is a schematic diagram of the generation of Bias\_Mid voltage, according to an embodiment of the invention.
- [0024] Figure 9B is a schematic diagram of an alternative embodiment for the generation of Bias\_Mid voltage, according to an embodiment of the invention.
- [0025] Figure 9C is a schematic diagram of yet another alternative embodiment for generation of Bias\_Mid voltage, according to an embodiment of the invention.
- [0026] Figure 10 is a schematic diagram of an exemplary well biasing circuit, according to an embodiment of the invention.
- [0027] Figure 11A is a schematic diagram of a circuit used to generate  $V_{GP1}$ .
- [0028] Figure 11B is a schematic diagram illustration of the generation of  $V_{DDO} - V_{TP}$  depicted in figure 11A.
- [0029] Figure 11C is a graph illustrating the relationship between Bias\_Mid and  $V_{PAD}$  according to an embodiment of the invention.
- [0030] Figure 11D is a schematic diagram depicting an exemplary illustration of a transistor implementation of block 901.
- [0031] Figure 12 is a schematic diagram of a circuit that may be used to prevent power on stress of devices, according to an embodiment of the invention.

[0032] Figure 13 is a circuit and block diagram of a portion of an over voltage protection circuit.

[0033] Figure 14 is a schematic diagram illustrating a modification of Figure 9A.

[0034] Figure 15 is a schematic diagram illustrating a transistor implementation of block 1401.

[0035] Figure 16 is a schematic diagram illustrating a transistor implementation of Figure 14.

[0036] Figure 17 is a schematic diagram of a circuit that may be used to prevent stress on devices when voltage spikes appear at an I/O pad.

[0037] Figure 18 is a schematic diagram of a circuit including several previously illustrated embodiments of the invention.

[0038] Figure 19 is a schematic diagram of a circuit that provides proper biasing of the I/O circuit when in power management mode, *i.e.*, when one or more of the power supply voltages are powered off.

[0039] Figure 20 is a transistor implementation of an alternate embodiment of block 901 of the circuit depicted in Figure 16 of this disclosure.

[0040] Figure 21 is a transistor implementation of an alternate embodiment of block 1401 of the circuit depicted in Figure 16 of this disclosure.

[0041] Figure 22 is a transistor implementation of an alternate embodiment of block 405 and 401 of the circuit depicted in Figure 6 of this disclosure.

#### DETAILED DESCRIPTION OF THE INVENTION

[0042] Figure 1 is a graphic illustration of an exemplary environment in which embodiments of the invention may be utilized. In Figure 1 a personal computer system is represented generally at 101. Within the computer system is circuit board 103 on which a CPU integrated circuit chip 105 is mounted. The CPU is a type which uses 3.3 volts as its supply voltage. A keyboard interface integrated circuit chip 107 is also mounted on circuit board 103. The keyboard interface integrated circuit uses a supply voltage of 5.0 volts. The

CPU 105 is coupled to the Keyboard chip 107. The CPU 105 may be of a type which contains integrated devices that may be damaged by interfacing with a device having a higher supply voltage. Because of the disparity in supply voltages that may exist in such situations an output circuit which can compensate for the higher interface voltages may be useful.

[0043] Figure 2 is a graphical illustration of a prior art input output circuit and connection. A common input output circuit comprises a pull up device, such as PMOS (P-channel Metal Oxide Semiconductor) device 215 and a pull down device, such as NMOS (N-channel Metal Oxide Semiconductor) device 217, such as illustrated in Figure 2. Devices 215 and 217 are coupled together at an input/output (I/O) pad 219. The substrate for the NMOS device is commonly coupled to ground potential, e.g. as shown at 221. The substrate for the PMOS device is typically a substrate which is common for the entire integrated circuit chip on which it resides. PMOS devices are commonly fabricated in their own isolated well.

[0044] Circuit 105 is an inverting push/pull device. An information signal is received at the gates 211 and 205 of transistors 215 and 217. If the signal at gates 211 and 205 is high, then NMOS device 217 will conduct and the I/O pad 219 will be pulled to the low reference voltage. If the signal at gates 211 and 205 is low, then PMOS device 215 will conduct, and the I/O pad 219 will be pulled to the high reference voltage Vdd.

[0045] In deep submicron fabrication, the component integrated devices can tolerate only limited differential voltages across their junctions. Commonly the voltage which can be tolerated across the junctions is on the order of 2.5 Volts.

[0046] In the illustration of Figure 2, pad 219 interfaces to a 5 volt circuit, and hence the pad may commonly see voltages in the neighborhood of 5.5 volts. A 5 volt signal applied to pad 219 may stress devices within the chip 105. For example if gate 205 of device 217 is at a zero volt potential then the voltage across the 205-203 gate-oxide can exceed 5 volts, thereby stressing device



217. For this reason more than one device may be used to divide the voltages in pull up and pull down I/O circuits.

[0047] Figure 3 is a schematic of a portion of a MOS (Metal Oxide Semiconductor) input output circuit in which each push pull output device illustrated in Figure 2 has been replaced by two devices. That is output device 215 has been replaced by devices 301 and 303 and device 217 has been replaced by devices 305 and 307. By replacing devices 215 and 217 by two devices each, the output voltage appearing at pad 309 may be safely divided over the two upper (301 and 303) and the two lower (305 and 307) I/O devices. The middle NMOS device 303 and the middle PMOS device 305 have their gates biased to intermediate potentials to avoid excessive voltages under various I/O pad, 309, voltages. Thus, devices 301 and 307 serve to drive the signal at the I/O pad 309, while devices 303 and 305 protect devices 301 and 307 by having their gates biased to intermediate voltages.

[0048] Figure 4 is an input output circuit 404, including a well biasing circuit, according to an embodiment of the invention. Devices 301 and 303 are fabricated in wells, illustrated schematically as 400 and 402, which are essentially at a floating potential. Because devices in wells at floating potential can have problems, such as device latch up, wells may commonly be coupled to a known bias voltage. The wells of devices 301 and 303 are coupled to the highest circuit potential available using well biasing circuit 401. The inputs to the well biasing circuit are the pad voltage present on input output pad 309, voltage  $V_{DDO}$  and bias voltage  $V_{GPI}$  which are illustrated in figure 7.

[0049] During the operation of input output circuit 404 in an output mode (when pad 309 is in an output driving mode), wells 400 and 402 are coupled to voltage  $V_{DDO}$ . When the pad 309 is in an input mode, the well voltage depends upon the I/O pad voltage. In the output enable mode  $V_{well} = V_{DDO}$ .

[0050] When input output circuit 404 is in an input mode (when pad 309 is in an input mode),  $V_{well}$  depends on both the input (Pad) voltage  $V_{PAD}$  and  $V_{DDO}$ . If  $V_{PAD}$  is less than  $V_{DDO}$  when the input output circuit 404 is in the input

mode, then  $V_{\text{well}} = V_{\text{DDO}}$ . If  $V_{\text{PAD}}$  is greater than  $V_{\text{DDO}}$  then  $V_{\text{well}} = V_{\text{PAD}}$ . A graph of this relationship is illustrated in Figure 5.

[0051] Figure 5 is a graph illustrating the relationship between well voltage and pad voltage for the I/O circuit in an input (or a tristate) condition. As can be seen from the graph, if the pad voltage is less than  $V_{\text{DDO}}$ , then the well voltage is equal to  $V_{\text{DDO}}$ . If the pad voltage is greater than  $V_{\text{DDO}}$ , then the well voltage is equal to the pad voltage. The well bias can thereby be changed according to changing circuit conditions.

[0052] Figure 6 is a block diagram of I/O circuitry 600 biasing according to an embodiment of the invention. When I/O circuitry 600 is in the input mode, first bias circuit 407 ties gate 403 of device 301 to  $V_{\text{DDO}}$ . In the output mode device 301 is controlled by an input from first bias circuit 407 according to whether a high or low value is the desired output on the pad 309.

[0053] In the input mode second bias circuit 405 provides gate voltage  $V_{\text{GP1}}$  to the gate of output device 303. The gate voltage  $V_{\text{GP1}}$  provided to the gate of output device 303 varies from an intermediate power supply voltage, such as  $V_{\text{DDC}}$  being equal to 1.2 volts, and the pad voltage presented to the circuit at input output pad 309. Such biasing prevents device 303 from being damaged due to a voltage potential across its junctions larger than the allowed maximum voltage of the device.

[0054] Figure 7 is a graphical representation of  $V_{\text{GP1}}$  bias voltage as a function of pad voltage ( $V_{\text{PAD}}$ ). If  $V_{\text{PAD}}$  is less than  $V_{\text{DDO}}$ , then  $V_{\text{GP1}}$  provided to the gate of output device 303 is equal to the intermediate supply voltage  $V_{\text{DDC}}$ . If  $V_{\text{PAD}}$  is greater than  $V_{\text{DDO}}$  then  $V_{\text{GP1}}$  provided to the gate of output device 303 is equal to  $V_{\text{PAD}}$ . In such a manner the voltage between the gate of device 303 and pad 309 can be kept in a safe range to prevent damage to the junction.

[0055] To summarize the operation of the circuit of Figure 6, when the circuit 600 is in an output mode, the well biasing circuit 401 ties the wells of devices 301 and 303 to  $V_{\text{DDO}}$ . The gate of the lower PMOS device 307 is tied to an

intermediate voltage, such as  $V_{DDC} = 1.2$  Volts. The gate of upper NMOS device 305 is tied to an intermediate voltage, such as  $V_{DDP} = 2.5$  Volts.

[0056] When the circuit 600 is in not in output mode, that is in the tri-state or input mode then upper PMOS device 301 and lower NMOS device 307 are turned off and the gates of devices 303 and 305 are driven to voltages which will not damage the circuit while the pad 309 is being driven by an external bus.

[0057] The gate voltage of the upper NMOS device 305 is controlled by third bias circuit 409. Third bias circuit 409, when in an input or tristate mode, will increase the bias voltage when the pad voltage increases beyond a certain threshold, for example  $V_{DDP}$  equal to 2.5 Volts.

[0058] Fourth bias circuit 411 works in a similar fashion to first bias circuit 407. Both bias circuits 407 and 411 work in a digital mode, either providing a first or second voltage depending on the required I/O pad 309 output voltage. In a first mode of operation first bias circuit 407 switches between a first voltage  $V_{DDO}$  and a second lower voltage  $V_{DDC}$ . Gate bias circuit 411 switches between providing  $V_{DDP}$  and ground potential to the gate of device 307.

[0059] Figure 8 is a circuit configuration used to provide the pad voltage to the core circuitry. The  $V_{PAD}$  input is coupled to the core circuitry 803 through an NMOS device 801. The gate of NMOS device 801 accepts Bias\_Mid as its control voltage. Such an arrangement protects the gate source voltage of device 801 and also prevents large voltages from the input from being coupled into the core circuitry when it is in the input, (tristate) or output conditions.

[0060] One facet of the I/O system comprising devices 301, 303, 305 and 307 is that any number of such devices may be added in parallel, in order to provide any level of drive signals needed.

[0061] Figure 9A is a schematic diagram illustrating how Bias\_Mid voltage is generated. Circuit 901 is a switching circuit that switches its Bias\_1 output between voltages  $V_{DDO}$  (3.3 Volts nominally in one embodiment) and  $V_{DDC}$  (1.2 Volts nominally in one embodiment). Device 905 is a PMOS device as are devices 907 and 909. Device 907 turns on when the output is enabled or

the  $V_{PAD}$  is low. When device 907 is turned on, Bias\_Mid is coupled to  $V_{DDP}$ . When output is not enabled i.e. the pad is in the tri-state (input only) mode and  $V_{PAD}$  is high, then Bias\_1 is equal to  $V_{DDO}$  and device 905 charges point 911 to Bias\_1 minus  $V_{TP}$ , where  $V_{TP}$  is the threshold of device 905, and accordingly is the voltage dropped across device 905. If Bias\_Mid is greater than the sum of  $V_{DDP}$  and  $V_{TP}$ , then device 909 will drain current from node 911 such that the sum of  $V_{DDP}$  plus  $V_{TP}$  is the maximum value for Bias\_Mid. Bias\_Mid is always between  $(V_{DDP} + V_{TP})$  and  $(V_{DDO} - V_{TP})$ , whether  $(V_{DDP} + V_{TP})$  or  $(V_{DDO} - V_{TP})$  is larger. A typical value of the threshold voltage  $V_{TP}$  is .5 volts. The actual value of Bias\_Mid will be determined by the relative sizes of devices 907 and 909.

[0062] Figure 9B is a schematic diagram of an alternate embodiment illustrating how Bias\_Mid voltage is generated in an alternate embodiment. Circuit 901 is a switching circuit that switches its Bias\_1 output between voltages  $V_{DDO}$  (3.3 Volts nominally in the present embodiment) and  $V_{DDC}$  (1.2 Volts nominally in the present embodiment). Device 905 is a PMOS device as is device 907. Device 909B is a NMOS device. Device 907 turns on when the output is enabled or the  $V_{PAD}$  is low. When device 907 is turned on, Bias\_Mid is coupled to  $V_{DDP}$ . When output is not enabled i.e. the pad is in the tri-state (input only) mode and during this time when  $V_{PAD}$  is high, then Bias\_1 is equal to  $V_{DDO}$  and device 905 charges point 911 to Bias\_1 minus  $V_{TP}$ , where  $V_{TP}$  is the threshold of device 905, and accordingly is the voltage dropped across device 905. If Bias\_Mid is greater than the sum of  $(V_{DDP} + V_{TP})$  then device 909b will drain current from node 911 such that  $(V_{DDP} + V_{TP})$  is the maximum value for Bias\_Mid. Bias\_Mid is always between  $(V_{DDP} + V_{TN})$  and  $(V_{DDO} - V_{TP})$ , whether  $(V_{DDP} + V_{TN})$  or  $(V_{DDO} - V_{TP})$  is larger. A typical voltage value for the threshold voltage  $V_{TP}$  is .5 volts. The actual value of Bias\_Mid will be determined by the relative sizes of devices 907 and 909b.

[0063] Figure 9C is a schematic diagram of yet another alternate embodiment for generation of Bias\_Mid voltage. In this circuit Bias\_Mid is always greater than  $(V_{DDP} + V_{TN})$  and less than  $(V_{DDO} - V_{TP})$ .

[0064] Figure 10 is a schematic diagram of an exemplary well biasing circuit, according to an embodiment of the invention. Device 1001, when turned on, couples the I/O pad 309 to the well 1005. Device 1003, when turned on, couples  $V_{DDO}$  to the well 1005. When  $V_{PAD}$  is less than  $V_{DDO}$  the gate source of device 1001 is less than the threshold voltage of device 1001, and device 1001 is turned off. When  $V_{GP1}$  is low (e.g. 1.2 Volts) then device 1003 conducts, thereby tying the well 1005 to  $V_{DDO}$ . When  $V_{PAD}$  is equal to  $V_{DDO}$  or greater then device 1001 will begin to turn on, thereby coupling the well 1005 to  $V_{PAD}$ .

[0065] Figure 11A is a schematic diagram of a circuit used to generate  $V_{GP1}$ . Bias\_1 switches between  $V_{DDO}$  (3.3 volts) and  $V_{DDC}$  (1.2 volts). Device 1101 couples Bias\_1 to  $V_{GP1}$ . When bias\_1 is 3.3 volts device 1101 couples 3.3V to  $V_{GP1}$ , and when bias\_1 is 1.2 Volts then,  $V_{GP1}$  is tied to 1.2 volts. When the  $V_{PAD}$  at 309 is greater than  $V_{DDO}$  device 1103 begins to conduct, because the gate of device 1103 is tied to  $(V_{DDO}-V_{TP})$ , and  $V_{GP1}$  is thereby coupled to  $V_{PAD}$ .

[0066] Figure 11B shows a circuit which may be used to generate  $(V_{DDO} - V_{TP})$ . The strong upper PMOS device charges the node 1150 to  $(V_{DDO} - V_{TP})$ . In addition to the problems that may be caused when a lower supply voltage chip is interfaced with a higher voltage chip "power-on stress" problems, which may be caused when circuitry is turned on and the supplies that provide protective biases are not yet up to their full voltage, may exist. In such a case a voltage present at an I/O pad may stress devices which are coupled to that I/O pad.

[0067] Figure 11C is a graph illustrating the relationship between Bias\_Mid and  $V_{PAD}$ . Bias\_Mid is set at 2.5 volts, and remains at 2.5 volts until  $V_{PAD}$  increases beyond 2.5 volts. Thereafter Bias\_Mid tracks increases with  $V_{PAD}$  and becomes equal to a higher voltage when  $V_{PAD}$  increases beyond a certain value.

[0068] Figure 11D is a schematic diagram depicting an exemplary illustration of a transistor implementation of circuit 901.

[0069] Figure 12 is a schematic diagram of a circuit that may be used to prevent power on stress of devices, according to an embodiment of the invention. The circuit illustrated in figure 12 may be used to generate the Bias\_Mid voltage when  $V_{DDO}$  is not up to its nominal value. If Bias\_Mid is present then devices 301, 303, 305 and 307, shown in figure 8, will be protected from junction over voltage problems even though the voltages, which ordinarily would be used to generate Bias\_Mid as explained in figure 9, are not present *e.g.*, in power management mode.

[0070] In Figure 12 devices 1201a-g are arranged as a series of diode coupled PMOS transistors such that a threshold voltage  $V_{TP}$  (in the present example equal to approximately .5 volts) is dropped across each device when it is conducting. Devices 1203a-h are similarly arranged diode coupled NMOS transistors. A threshold voltage  $V_{TN}$  is dropped across 1203a-h if Bias\_Mid is high.

[0071] Device 1207, in essence, acts as a switch. If  $V_{DDO}$  is not present, then device 1215 turns off, device 1221 conducts, and the gate of device 1207 is pulled high. This causes device 1207 to conduct. Similarly, if  $V_{DDP}$  is not present, then device 1217 turns off, device 1223 conducts, and the gate of device 1207 is again pulled high. This also causes device 1207 to conduct. When device 1207 is conducting, the pad voltage, minus the threshold voltage of devices 1201a-g, is coupled to Bias\_Mid.

[0072] If  $V_{DDO}$  and  $V_{DDP}$  are present, then devices 1215 and 1217 will conduct, and the gate of device 1207 is pulled low to  $V_{DDC}$ . This causes device 1207 to turn off. As a result, if  $V_{DDO}$  or  $V_{DDP}$  are not present, as in power management mode, then the circuit depicted in FIG. 12 will supply Bias\_Mid using only  $V_{PAD}$ .

[0073] Figure 13 is a circuit and block diagram of a portion of an over voltage protection circuit. Device 1001 provides a protection mechanism for the well bias. If the pad voltage is higher than  $V_{DDO}$  is lower than by  $V_{TP}$  or more, then device 1001 will turn on. If device 1001 turns on then the well is coupled, via device 1001, to the pad, and hence the well will be biased to  $V_{PAD}$ .

[0074] Similarly device 1301 is coupled between the pad and P\_Gate, the gate of PMOS device 303 shown in figure 6. The gate of device 1301 is biased so that when the pad voltage 309 is higher than  $V_{DDO}$  by  $V_{TP}$  or more, then device 1301 will turn on and couple P\_Gate to the pad voltage, therefore if  $V_{DDO}$  is low then P\_Gate will not depend on  $V_{DDO}$  for it's voltage level and instead will take the voltage level from the voltage on the pad.

[0075] Figure 14 is a schematic diagram illustrating a modification of Figure 9. In Figure 14 circuit 901 is decoupled from the Bias\_Mid signal when  $V_{DDO}$  is lower than its nominal value. The decoupling is done by using circuit 1401. When  $V_{DDO}$  is not up to its nominal value, the node  $V_{pwr}$  is decoupled from  $V_{DDP}$  by using circuit 1401 as a switch. When  $V_{DDO}$  is up to its nominal value, the node  $V_{pwr}$  is coupled to  $V_{DDP}$  by using circuit 1401.

[0076] Figure 15 is a schematic diagram illustrating a transistor implementation of circuit 1401. When  $V_{DDO}$  is greater than a certain value, NMOS 1507 is turned on thereby connecting the gate of PMOS 1505 to  $V_{DDC}$ . Connecting the gate of PMOS 1505 to  $V_{DDC}$  turns on 1505 thereby connecting  $V_{pwr}$  to  $V_{DDP}$ . When  $V_{DDO}$  is less than a certain value, NMOS 1507 is turned off and PMOS 1506 is turned on thereby connecting the gate of PMOS 1505 to Bias\_Mid, thereby turning off PMOS 1505 and disconnecting  $V_{pwr}$  from  $V_{DDP}$ .

[0077] Figure 16 is a schematic diagram illustrating a transistor implementation of the circuitry illustrated in Figure 14.

[0078] Figure 17 is a schematic diagram of a circuit that may be used to prevent stress on devices when voltage spikes appear at an I/O pad. When transient voltages appear, the Bias\_Mid voltage changes momentarily due to the gate to drain overlap capacitance ( $C_{gd}$ ) of the driver NMOS. A capacitance ( $C_{bm}$ ) is placed at the bias\_mid node such that the transient voltage at the pad ( $V_{pad,transient}$ ) gets divided between  $C_{gd}$  and  $C_{bm}$  depending on the ratio of the capacitances which gives the additional transient voltage on bias\_mid( $V_{bm,transient}$ ):

$$\Delta V_{\text{bm,transient}} = (C_{\text{gd}}/(C_{\text{gd}}+C_{\text{bm}})) * \Delta V_{\text{pad,transient}}.$$

[0079] Also, when transient voltages appear, the voltage  $V_{\text{GP1}}$  on PMOS 207 gate changes momentarily due to the gate to drain overlap capacitance ( $C_{\text{gdp}}$ ) of the driver PMOS. A capacitance ( $C_{\text{gp}}$ ) is placed at the PMOS 207 gate node such that the transient voltage at the pad ( $V_{\text{pad,transient}}$ ) gets divided between  $C_{\text{gdp}}$  and  $C_{\text{gp}}$  depending on the ratio of the capacitances which gives the additional transient voltage on PMOS 207 gate ( $V_{\text{GP1+transient}}$ ):

$$\Delta(V_{\text{GP1+transient}}) = (C_{\text{gdp}}/(C_{\text{gdp}}+C_{\text{gp}})) * \Delta(V_{\text{pad,transient}}).$$

[0080] Figure 18 is a schematic diagram of a circuit including several previously illustrated embodiments of the invention. The transistors illustrated in figure 18 are all 2.5 volt devices. The maximum output pad voltage is 3.6 volts and the maximum input voltage on  $V_{\text{PAD}}$  309 is 5.5 volts. The typical values of power supplies are  $V_{\text{DDO}} = 3.3$  volts,  $V_{\text{DDP}} = 2.5$  volts,  $V_{\text{DDC}} = 1.2$  volts,  $V_{\text{SSC}} = 0$  volts and  $V_{\text{SSO}} = 0$  volts. The operation of the circuit of figure 18 under various operating conditions is summarized below.

[0081] When the I/O pad 309 is in an output enabled mode (i.e. OE is high) the maximum pad voltage is  $V_{\text{DDO}}$ .  $V_{\text{GP1}}$  at the gate of PMOS device 303 is coupled to  $V_{\text{DDC}}$  through NMOS transistors 1101 and 1801 and accordingly PMOS device 303 is turned on. Circuit 901 generates an output Bias\_1 voltage of  $V_{\text{DDC}}$  and accordingly PMOS device 907 is turned on, the steady state voltage of Bias\_Mid is  $V_{\text{DDP}}$  and PMOS device 905 is turned off.

[0082] When the I/O pad 309 is output disabled (i.e. OE is low) and the pad voltage is below a predetermined value, then  $V_{\text{GP1}}$  at the gate of PMOS 303 is floating if the pad voltage is below  $V_{\text{DDO}}$ . Circuit 901 generates a output Bias\_1 voltage of  $V_{\text{DDC}}$  and accordingly PMOS device 907 is turned on, the steady value of Bias\_Mid voltage is  $V_{\text{DDP}}$ , and PMOS device 905 is turned-off in this condition.



[0083] When the I/O pad 309 is output disabled (i.e. OE is low) and the pad voltage is above a predetermined value, then circuit 901 generates an output Bias\_1 voltage of  $V_{DDO}$  and accordingly PMOS device 907 is turned-off, PMOS device 905 is turned on, and the steady state value of Bias\_Mid is between  $(V_{DDO} - V_{TP})$  as a minimum value and  $(V_{DDP} + V_{TN})$  as a maximum value, where  $V_{TP}$  and  $V_{TN}$  are offset voltages due to the turn on threshold voltages of transistors 905 and 909b respectively.  $V_{GP1}$ , at the gate of PMOS device 303 is coupled to the pad voltage if the pad voltage is greater than  $V_{DDO}$ .

[0084] Capacitors  $C_{bm}$  and  $C_{gp}$  in figure 18 are used to insure that Bias\_Mid voltage and  $V_{GP1}$  voltage, respectively, are kept at desirable levels when transient voltages appear at the pad as was described relative to Figure 17.

[0085] Figure 19 is a schematic diagram of a circuit that provides proper biasing of protective devices 303 and 305 regardless of whether the circuit is in power management mode, or in a normal mode of operation. In power management mode, one or more of the plurality of power supplies (e.g.,  $V_{DDO}$ ,  $V_{DDP}$  and  $V_{DDC}$ ) are powered off.

[0086] As explained above, devices 301 and 303 represent the pull-up section of the I/O circuit, while devices 305 and 307 represent the pull-down section. Devices 301 and 307 are the signal driving devices, while devices 303 and 305 are the protective devices, which are biased to intermediate voltages to protect the I/O circuit from high transient voltages that could damage the I/O circuit. Circuits 1911 and 1917 represent the pre-drivers for devices 301 and 307 respectively.

[0087] In an exemplary embodiment, and as noted above, the plurality of power supplies have the following nominal values:  $V_{DDO} = 3.3$  volts,  $V_{DDP} = 2.5$  volts,  $V_{DDC} = 1.2$  volts,  $V_{SSC} = 0$  volts and  $V_{SSO} = 0$  volts. These supply voltages and the associated circuitry described above, are used to bias protective devices 303 and 305. As described above, Bias\_Mid is the bias voltage applied to protective NMOS device 305, while  $V_{GP1}$  is the bias voltage applied to protective PMOS device 303. When one or more of the supply

voltages are off, (e.g., when circuit is in power management mode) the present invention ensures that protective devices 303 and 305 are properly biased to maintain tolerable voltage stress across the gate oxides and junctions and to keep the leakage current substantially below  $1\mu\text{A}$ . Proper biasing is accomplished using the I/O pad voltage 309 to generate Bias\_Mid and  $V_{\text{GP1}}$ . This method and circuit for normal operation and power management mode are described below.

[0088] In normal mode, reference circuit 1901 is an alternate transistor implementation of circuit 901. Reference circuit 1901 provides a reference input to switch 1950 for generation of bias voltage Bias\_Mid during normal operation in input and output modes. Depending on the reference voltage from circuit 1901, Bias\_Mid toggles between  $V_{\text{DDO}}$  and  $V_{\text{DDP}}$ . Reference circuit 1901 also provides bias voltage  $V_{\text{GP1}}$  (i.e., the gate of protective device 303) via switch 1955 as long as  $V_{\text{DDO}}$  is present. As is explained in more detail below, as long as supply voltages  $V_{\text{DDO}}$ ,  $V_{\text{DDP}}$  and  $V_{\text{DDC}}$  are present, reference bias circuit 1901, in combination with switches 1950 and 1955, generate bias voltages Bias\_Mid and  $V_{\text{GP1}}$  to properly bias protective devices 305 and 303 respectively.

[0089] In power management mode, where one or more power supply voltages are not present, an alternate method of biasing protective devices 303 and 305 is needed. An alternate biasing scheme is provided by self-bias circuits 1960 and 1940, which generate bias voltages Bias\_Mid and  $V_{\text{GP1}}$  using only the voltage present at the pad 309. Accordingly, when one or more supply voltages are off (e.g., in power management mode), switches 1950 and 1955 essentially de-coupled bias circuit 1901 from self-bias circuits 1960 and 1940. As described below, self-bias circuit 1960 is used to generate Bias\_Mid with only the I/O pad voltage ( $V_{\text{PAD}}$ ) 309. As also described below, self-bias circuit 1940 receives Bias\_Mid and generates  $V_{\text{GP1}}$  in power management mode. Self-bias circuit 1940 also provides the bias for the floating well for devices 301 and 303 in all modes of operation, including power management mode.

[0090] Figure 20 is one embodiment of reference circuit 1901, which generates voltages bias\_1b and bias\_1 in normal mode. In the normal mode, pass transistor devices 2001 and 2002 protect reference circuit 1901 from excessive I/O pad voltage. If  $V_{PAD}$  309 rises above the voltage Bias\_Mid, then device 2001 will charge node 2090 to Bias\_Mid minus the threshold voltage of device 2001, thus protecting device 2001 from overstress. Similarly, if  $V_{PAD}$  309 rises above  $V_{DDP}$ , device 2002 will charge node 2091 to  $V_{DDP}$  minus the threshold voltage of device 2002, thus protecting device 2002 and inverter 2010 from overstress.

[0091] While in normal mode, inverters 2010 and 2020 act as buffers between the I/O pad voltage 309 and comparator 2040. Inverter 2020 is controlled by output enable signal ("oes"), generated by output enable circuit 2050. If "oes" is low, inverter 2020 will invert the output of inverter 2010. If "oes" is high, the output of inverter 2020 is low. The input of output enable circuit 2050 is "oeb" and is either an external, user defined input, or an internally generated signal. Inverter 2030 coupled the gates of NMOS transistors 2041 and 2043 of comparator 2040. The gates of PMOS transistors 2042 and 2044 are cross connected to each others sources.

[0092] Still in the normal mode, where  $V_{PAD}$  309 is in normal operating range (e.g., 0-3.3V) bias\_1b and bias\_1 will toggle between  $V_{DDO}$  and  $V_{DDC}$ , depending on the I/O pad voltage. For example, where  $V_{PAD}$  is HIGH, output of inverter 2010 is LOW, and output of inverter 2020 is HI. As a result, a HIGH signal is at the gate of NMOS transistor 2041, causing transistor 2041 to conduct, while inverter 2030 puts a LOW signal to the gate of NMOS transistor 2043, causing transistor 2043 to turn off. Thus, bias\_1b is equal to  $V_{DDC}$  (e.g., 1.2V). This, in turn, puts  $V_{DDC}$  at the gate of PMOS transistor 2044, causing it to conduct. As a result, bias\_1 is equal to  $V_{DDO}$  (e.g., 3.3V), which also ensures that PMOS transistor 2042 is off. If  $V_{PAD}$  is LOW, the reverse is true and bias\_1 goes to  $V_{DDC}$  (e.g., 1.2V), while bias\_1b goes to  $V_{DDO}$  (e.g., 3.3V).

[0093] In power management mode, one or more supply voltages  $V_{DDO}$ ,  $V_{DDC}$  and  $V_{DDP}$  are powered off. In this state, the output of reference circuit 1901 is low—*i.e.*, both  $\text{bias\_1}$  and  $\text{bias\_1b}$  are low. As is explained in more detail below with respect to FIG. 21, reference circuit 1901 is effectively de-coupled from  $\text{Bias\_Mid}$  and  $V_{GP1}$  in power management mode by switches 1950 and 1955.

[0094] Figure 21 is a transistor implementation of switches 1950, 1955 and self-bias circuit 1960. Switch 1950 is one embodiment of circuit 1401. In normal mode, switch 1950 receives  $\text{bias\_1b}$  and  $\text{bias\_1}$  at the gates of PMOS transistors 2150 and 2152 respectively. If  $\text{bias\_1b}$  is LOW (*e.g.*,  $\text{bias\_1b} = V_{DDC} = 1.2\text{ V}$ , where  $V_{PAD}$  is HIGH), PMOS transistor 2150 is on, and  $V_{DDO}$  (*e.g.*,  $3.3\text{ V}$ ) is supplied to  $\text{Bias\_Mid}$ . If  $\text{bias\_1}$  is LOW (*e.g.*,  $\text{bias\_1} = V_{DDC} = 1.2\text{ V}$ , where  $V_{PAD}$  is LOW), PMOS transistor 2152 is on, and intermediate supply voltage  $V_{DDP}$  (*e.g.*,  $2.5\text{ V}$ ) is supplied to  $\text{Bias\_Mid}$ .

[0095] In power management mode, switch 1950 isolates reference circuit 1901 and power supplies  $V_{DDO}$  and  $V_{DDP}$  from self bias circuit 1960. Where  $V_{DDO}$  and  $V_{DDP}$  are powered off, the gates of 2151 and 2154 are tied up to  $\text{Bias\_Mid}$ . This causes transistors 2151 and 2154 remain off. Thus, transistors 2151 and 2154 serve to de-couple  $V_{DDO}$  and  $V_{DDP}$ , as well as circuit 1901, from  $\text{Bias\_Mid}$ . In this fashion, circuit 1950 can be modeled as a switch that is responsive to reference voltages from reference circuit 1901, as well as to supply voltages  $V_{DDO}$  and  $V_{DDP}$ .

[0096] Circuit 1955 also acts as a switch in power management mode. Ordinarily,  $\text{bias\_1}$  is supplied to  $V_{GP1}$  through circuit 1955. However, because NMOS transistor 2155 has its gate tied to reference voltage  $V_{DDO}$ , it conducts when  $V_{DDO}$  is at its nominal value of  $3.3\text{ V}$ , and is off if supply voltage  $V_{DDO}$  is off. Therefore,  $\text{bias\_1}$  is not supplied to  $V_{GP1}$  when in power management mode, since  $V_{DDO}$  is powered off. In this fashion, circuit 1955 can also be modeled as a switch that is responsive to reference voltages from reference circuit 1901, as well as supply voltage  $V_{DDO}$ .

[0097] Self-bias circuit 1960 generates Bias\_Mid when the I/O circuit is in power management mode, or when  $V_{PAD}$  is excessively high. In self-bias circuit 1960, it can be seen that Bias\_Mid will be represented by the following relationship:

$$(V_{SSC} + nV_{TN}) > \text{Bias\_Mid} > (V_{PAD} - kV_{TP})$$

where  $V_{TN}$  is the threshold voltage for NMOS devices,  $n$  is the number of NMOS devices 2161-2163 connected in series between Bias\_Mid and  $V_{SSC}$  (ground or 0V),  $V_{TP}$  is the threshold voltage for PMOS devices, and  $k$  is the number of PMOS devices 2162-2164 connected in series between Bias\_Mid and  $V_{PAD}$ . In normal mode, transistor 2189 isolates transistor string 2162-2164 when supply voltages are present. Where  $V_{DDO}$  and  $V_{DDP}$  are present, transistors 2191 and 2193 both are on. This puts low voltage  $V_{DDC}$  at the gate of transistor 2189, turning it off. In power management mode, where  $V_{DDO}$  or  $V_{DDP}$  are off, PMOS transistors 2190 and 2192 conduct. This puts the voltage of the source of transistor 2189 at the gate of transistor 2189, thus making transistor 2189 act as a diode, allowing I/O pad voltage 309 to be dropped across the 250 ohm resistor and transistor string 2162-2164. Thus, in power management mode, Bias\_Mid depends only on the value of  $V_{PAD}$ , and does not rely on the plurality of supply voltages.

[0098] Figure 22 is a transistor implementation of self-bias circuit 1940, which is one embodiment of circuits 405 and 401 of the circuit depicted in Figure 6. In power management mode, self-bias circuit 1940 generates  $V_{GP1}$ . When the supply voltage  $V_{DDO}$  is powered off, PMOS transistors 2202 and 2204 both turn on. NMOS transistor 2201 turns off. As a result, PMOS transistor 2206 turns off and  $V_{DDO\_b}$  thus goes to Bias\_Mid that is generated by circuit 1960, which is applied to the gates of PMOS transistors 2242 and 2244. In this fashion, transistor 2202 acts as a switch isolating circuit 1960 from 1940 when  $V_{DDO}$  is present, and providing Bias\_Mid to circuit 1940 when  $V_{DDO}$  is absent.

[0100] Bias\_Mid is also applied to the gate of PMOS device 2246. Thus,  $V_{GP1}$  will depend on the value of both Bias\_Mid, which is supplied from self-bias circuit 1960, and  $V_{PAD}$ . If Bias\_Mid is sufficiently low compared to  $V_{PAD}$ , devices 2242 and 2246 will be on, and  $V_{GP1}$  will be equal to  $V_{PAD}$  dropped across the  $250\Omega$  resistor and PMOS transistors 2242 and 2246. Thus,  $V_{GP1}$  would be approximately equal to  $V_{PAD} - kV_{TP}$  wherein  $k$  is the number of said PMOS devices between transistors 2242 and 2246, and  $V_{TP}$  is the threshold voltage of said PMOS devices. Self-bias circuit 1940 also generates  $V_{WELL}$ .  $V_{WELL}$  is biased in all cases to the highest potential as between  $V_{DDO}$  and  $V_{PAD}$ . Such self-biasing prevents latch-up problems in PMOS devices 301 and 303. If Bias\_Mid is not sufficiently low compared to  $V_{PAD}$ , then  $V_{GP1}$  will be equal to  $V_{PAD}$  dropped across the  $3M\Omega$  resistor, as shown in FIG. 21.

## CONCLUSION

[0101] These embodiments are provided by way of example and not limitation. They describe an apparatus and method for properly biasing the I/O circuit when the plurality of reference voltages are powered off, *i.e.*, when the I/O circuit is in the power management mode. One skilled in the art would recognize other circuit designs that could implement the inventive concept of this disclosure.

[0102] Example embodiments of the methods, systems, and components of the present invention have been described herein. As noted elsewhere, these example embodiments have been described for illustrative purposes only, and are not limiting. Other embodiments are possible and are covered by the invention. Such other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.